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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,231	03/10/2004	Richard Hammond	ASC-057C1	2980

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EXAMINER	
GHYKA, ALEXANDER G	
ART UNIT	**PAPER NUMBER**
2812	

NOTIFICATION DATE	DELIVERY MODE
07/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/797,231	HAMMOND ET AL.	
	Examiner	Art Unit	
	ALEXANDER G. GHYKA	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/29/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicants' response of 4/29/2008 has been considered and entered in the record. Claims 28-55 are under consideration. With respect to the rejection of the prior Office action, the rejection of Claims 45-55 is withdrawn in view of Applicants' arguments. With respect to Claims 28-44, the rejection is maintained for the reasons as discussed below. **A new rejection is made in view of prior art cited by the Applicants**. Accordingly this Office action is a non-final rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 28-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ismail (Si/SiGe High Speed Field Effect Transistors, IEEE 1995) "Ismail" in view of Chang et al (Selective Etching of SiGe on SiGe/Si Heterostructures, J. Electrochem, Soc. Vol 138, No. 1, 1991 "Chang et al").

The present Claims generally require providing a strained semiconductor layer; providing a SiGe layer over said strained semiconductor layer; and selectively removing said SiGe layer to expose said strained semiconductor layer.

Ismail et al shows a FET formed providing a strained semiconductor layer; providing a SiGe layer over the strained semiconductor layer. See Figure 7, pg 20.01.03. The strained semiconductor layer comprises Si as required by present Claim 29. A relaxed semiconductor layer comprising Si and Ge is provided beneath the strained layer as required by present Claims 31-33. See Figure 7, page 20.1.3. With respect to Claims 34-35, Ismail discloses an insulator layer and exemplifies silicon dioxide. See last paragraph of column 1, page 20.1.3. With respect to Claims 40-44, Ismail discloses MOSFETs. See Figure 9, page 20.1.3.

However, Ismail does not disclose selectively removing the SiGe layer to expose the strained semiconductor layer.

Chang et al disclose a method for selectively removing SiGe disposed over Si by chemically oxidizing the SiGe to form a SiGe oxide in one region but not in another and then removing the oxidized SiGe. See page 202, columns 1 and 2 and page 203, Fig 4.

It would be obvious for one of ordinary skill in the art, at the time of the invention, to use the oxidation and etch method of Chang et al, to form the SiGe/Si structures of

Ismail, for their known benefit in the art of selectively removing the SiGe layer as disclosed by the Chang et al reference.

With respect to Claims 36-39, the oxidation and etch technique as required by the afore mentioned Claims, are disclosed by the Chang reference.

Response to Applicants' Arguments

Applicants argue that Ismail is utterly silent about any method utilized to form his structures of Figure 7 and 9, because he has not fabricated them. Applicants argue that Figures 7 and 9 are simply schematics of structures existing only in circuit performance models. The Examiner maintains that it would be obvious for one of ordinary skill in the art to make the model as shown by Ismail. The present method claims require "providing" and "removing" various layers. The fact that Ismail shows a model does not preclude the establishment of a *prima facie* case of obviousness, as it would be well within the skill of one of ordinary skill in the art to "provide" the layers as shown in the model of Ismail and arrive at the present Claims.

Applicants further argue that Ismail's structure may be fabricated in other ways, for example, rather than selectively removing layers from his N-MODFET structure, Ismail could add layers to his P-MODFET structure. The Examiner notes that simply because there are other ways of forming the device does not preclude the *prima facie* case of obviousness. Chang et al disclose a method for selectively removing SiGe disposed over Si by chemically oxidizing the SiGe to form a SiGe oxide in one region but not in another and then removing the oxidized SiGe. See page 202, columns 1 and

2 and page 203, Fig 4. It would be obvious for one of ordinary skill in the art to selectively remove layers as disclosed by Chang to arrive for the benefit of arriving at the structure as disclosed by Ismail. It would be obvious to one of ordinary skill in the art that to arrive at the device as illustrated by Ismail, one would have to selectively add or selectively remove SiGe. To do so by a process as disclosed by Chang is not "mere conjecture", but the use of a known method in the art for its known benefit. The burden in establishing a *prima facie* case of obviousness does not require that there be no other possibility to arrive at the present invention, but simply that it is obvious for one of ordinary skill in the art to do so. One of ordinary skill in the art, upon seeing the model of Ismail, would find it obvious to produce it by using the selective removal as disclosed by Chang et al.

Applicants argue that one of ordinary skill in the art would not utilize Chang's method to attempt to form Ismail's structure because Chang's approach would not achieve the straight vertical profile, and the resultant sidewall profile would be ragged and undercut. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., smooth lines) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993) . As noted by Applicants' Ismail is a model, and the present Claims do not require smooth sidewalls and merely require the selective removal of SiGe. With respect to the type of doping of the portion removed, Applicants's argue limitations

which are not in the claims. Moreover, Chang et al is not limited to one experiment. Furthermore, the Ismail reference is not limited to silicon dioxide insulators and it would be well within the skill of one of ordinary skill in the art to use another insulator.

The rejections of Claims 45-55 over Ismail and Chang are withdrawn in view of Applicants' arguments.

New Rejection in view of IDS of 4/29/2008

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 28-36, 39-40, 45-46 and 49-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Fitzgerald (US 6,646,322).

Fitzgerald discloses a relaxed silicon germanium platform for high speed CMOS electronics. Fitzgerald shows a FET formed providing a strained semiconductor layer; providing a SiGe layer over the strained semiconductor layer. See Figures 13A-13D and column 9, lines 20-45. The strained semiconductor layer comprises Si as required by present Claims 29, 49 and 50. See column 9, lines 31-33. A relaxed semiconductor

layer comprising Si and Ge is provided beneath the strained layer as required by present Claims 31-33 and 50-51. See Figure 13D. With respect to Claims 34-35 and 54, Fitzgeraldl discloses an insulator layer and exemplifies silicon dioxide. See Figure 10. With respect to Claims 36 and 39-40, Fitzgerald discloses thermal oxidation and wet etching. With respect to Claim 45, Fitzgerald discloses that the same strained Si layer 1306 provides the channel for both the surface and buried channel devices. See Figure 13D and corresponding text. With respect to Claim 46 Fitzgerald disclose source, drain and gate contact regions. See Figures 7C and 7D, and corresponding text.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 38-39 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitzgerald (US 6,646,322).

Fitzgerald is relied upon as disussed above.

However, Fitzgerald does not disclose the temperature of the thermal oxidation or specify p-type or n-type doping as required by the afore mentioned Claims.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to arrive at the presently claimed temperature range, as where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the

optimum or workable ranges by routine experimentation. See *Allen et al v. Coe,* 57 USPQ 136. Moreover, the discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. See *In re Antonie,* 195 USPQ 6 (CCPA 1977). In the present case the selection of the temperature range would be a matter of optimization for the benefit of optimizing the performance of the MOSFET. Moreover, with respect to the p-type and n-type implantation, Fitzgerald disclose implanting the source, drain and gate regions, and the selection of the type of dopant used would be obvious to one of ordinary skill in the art.

Claims 41-44 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fitzgerald (US 6,646,322) in view of Boyd et al (US 6,271,094).

Fitzgerald is relied upon as discussed above.

However, Fitzgerald does not disclose the use of a high k insulator in a MOSFET.

Boyd et al disclose a MOSFET which comprises a SIGe layer and the use of a high k dielectric layer. See column 2, lines 5-65 and column 9, lines 55-60.

It would have been obvious for one of ordinary skill in the art, at the time of the invention, to use a high k dielectric in the MOSFET of Fitzgerald, for its known benefit as an insulator in MOSFETs as disclosed by Boyd. The use of a known material, high k dielectric, for its known purpose, an insulator in a MOSFET would be within the skill of one of ordinary skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Friday during general business hours. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 3, 2008
AGG

ALEXANDER G. GHYKA

PRIMARY EXAMINER AU 2812

/Alexander G. Ghyka/